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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/634,851 | 08/06/2003 | Jun Kanamori | MAE 292 | 7005 |

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RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

| EXAMINER | |
|---|---|
| ISAAC, STANETTA D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/634,851 | KANAMORI, JUN | |
| | Examiner | Art Unit | |
| | Stanetta D. Isaac | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6,8-13 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the amendment filed on 3/3/05. Currently, claims 1-6, 8-13 and 17-20 are pending.

### *Information Disclosure Statement*

The information disclosure statement (IDS) was submitted on 6/18/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### *Specification*

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-13 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim US Patent 5,807,784 in view of Prabhakar US Patent 5,896,359.

Kim shows the semiconductor method substantially as claimed. See figures 1A-1B, 4A-4D, and corresponding text, pertaining to claims 1 and 8, where Kim shows a method of fabricating a semiconductor device, the method comprising: oxidizing a surface of the silicon substrate to form a pad oxide film **32** (figure 4A; col.5 lines 10-13); forming a first oxidation-resistant film **34** on the pad oxide film (figure 4A; silicon substrate **40**; col. 5, lines 10-13); selectively removing the first oxidation-resistant film from parts of the silicon substrate (figure 4A; col. 5, lines 1-9); implanting oxygen ions **37** through the pad oxide film and into selected parts of the silicon substrate, using the remaining parts of the first oxidation-resistant film as a mask (figure 4B; col. 5, lines 14-23); and oxidizing the selected parts of the silicon substrate (figure 4C; col. 5, lines 23-27), into which the oxygen ions have been implanted, and while the selected parts are still covered by the pad oxide film, to form isolation regions **38**, dividing the silicon substrate into a plurality of mutually isolated active regions (col. 5, lines 27-44, ***Note***: the Examiner takes the position that it is both inherent and well known that these techniques are used for isolation between devices). In addition, Kim shows, pertaining to claims 4 and 11, the method wherein the isolation regions are field oxide regions (figure 4C; col. 5, lines 38-44). Kim also shows, pertaining to claims 5, 6, 12 and 13, the method wherein the implanted oxygen ions have a concentration that varies from an upper surface of the silicon substrate to a lower surface of the silicon substrate and a peak concentration in a lower half of the silicon substrate (figures 4B- 4D; col. 5, lines 14-55, ***Note***: the Examiner takes the position that it is both inherent and well known that the implanted oxygen ions would have a concentration that varies from an upper and lower surface of the silicon substrate and a concentration in a lower half of the silicon substrate, since silicon conventionally includes an oxygen concentration at room temperature of

$2.5 \times 10^{15}/cm^3$. As a result, any additional oxygen ion implantation, within a specific region changes the concentration of the upper and lower surfaces of the substrate. See *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Second Edition, page 19, under 1.3.51 Oxygen and Carbon Measurements in Silicon Using Infrared Absorbance Spectroscopy*). Kim shows, pertaining to claim 17, wherein the first oxidation-resistant film **34** comprises at least one of a nitride film and a photoresist film (col. 5, lines 1-13). Finally, Kim shows, pertaining to claims 18 and 19, the method further comprising: depositing a second oxidation-resistant film **36** after the first oxidation-resistant film has been removed from the parts of the silicon substrate (figure 4A; col. 5, lines 1-9); and etching the second oxidation-resistant film to leave sidewalls on vertical edges of the remaining parts of the first oxidation-resistant film before the oxygen ions are implanted (figure 4A; col. 5, lines 1-9), wherein the second oxidation-resistant film is an oxide film or a nitride film (col. 5, lines 10-13, nitride layer).

However, Kim fails to show, pertaining to claims 1-6, 8-13 and 17-20, a method of fabricating a semiconductor device, having a silicon layer disposed on an insulating film where oxygen ions are implanted into the selective parts of the silicon layer and oxidized to form field oxide regions. In addition, Kim fails to show, pertaining to claim 20, providing a supporting substrate having an insulating film disposed thereon. Also, Kim fails to show, pertaining to claims 2 and 9, the silicon layer having a thickness of at most seventy nanometers. Kim also fails to show, pertaining to claims 3 and 10, wherein the semiconductor device is a fully depleted silicon-on-insulator device.

Prabhakar teaches in figures 1-10, and corresponding text, a semiconductor device, including field oxide regions formed within a silicon layer, pertaining to claims 1-6, 8-13 and 17-

20, a method of fabricating a semiconductor device, having a silicon layer (silicon on insulator (SOI)). Prabhakar also teaches, pertaining to claims 2 and 9, that the silicon layer has a thickness of at most seventy nanometers. Finally, Prabhakar teaches, pertaining to claims 3 and 10, the method wherein the semiconductor device is a fully depleted silicon-on-insulator device.

It would have been obvious to one of ordinary skill in the art to have incorporated, substituting the silicon substrate with the SOI substrate (providing a supporting substrate having an insulating film disposed thereon), implanting oxygen ions into selected parts of the silicon layer (with a thickness of at most seventy nanometers), and oxidizing the selected parts to form field oxide regions within the silicon layer where the completed device is a fully depleted SOI device, in the method of Kim, pertaining to claims 1-6, 8-13 and 17-20, according to the teachings of Prabhakar, with the motivation that, as stated in col. 1, lines 15-27; col. 4, lines 27-57, the fully depleted SOI device taught by Prabhakar, includes the use of field oxide regions formed within the selected parts of the silicon layer, where conventional technology teaches that these regions are used for the purpose of device isolation. In addition, one of ordinary skill in the art would be drawn to use of a thin SOI layer, taught in Prabhakar, with the motivation that, the SOI substrate produces lower parasitic capacitances for greater channel current, which in turns allows for faster switching speed.

***Response to Arguments***

Applicant's arguments with respect to claims 1-6, 8-13 and 17-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
May 14, 2005

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER